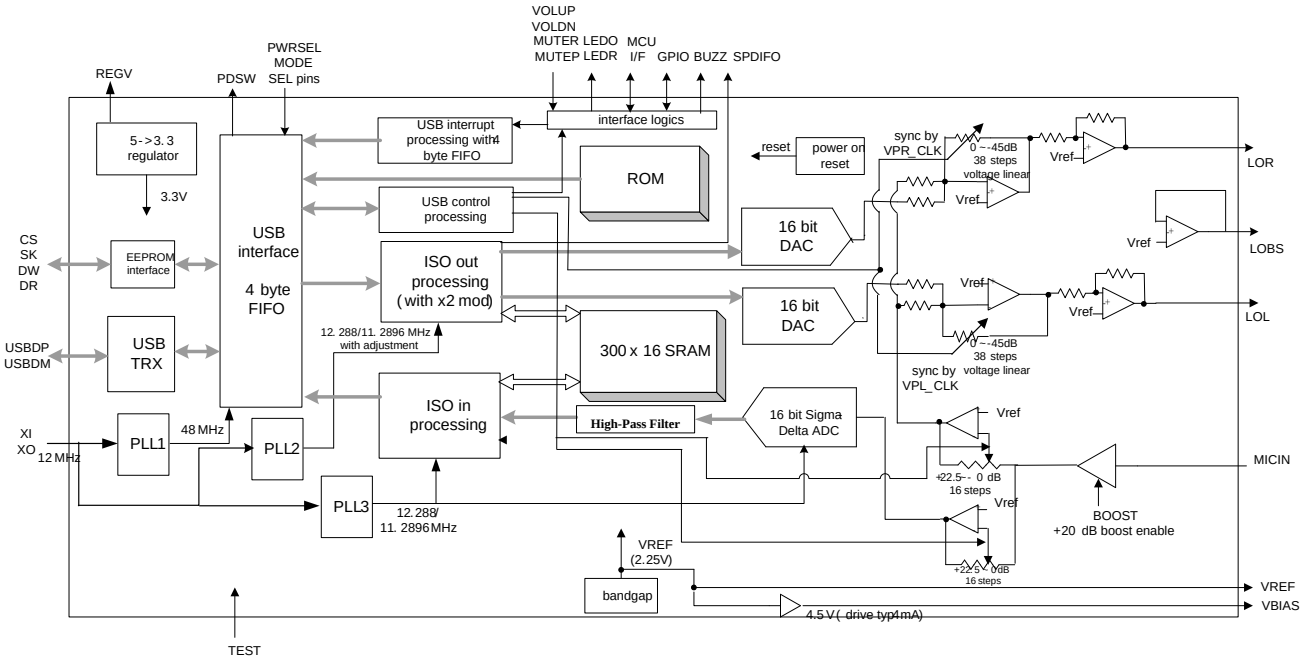
DESCRIPTION

The CM119A is a highly integrated single-chip USB audio controller specifically designed for VoIP (Voice over Internet Protocol) applications. All essential analog modules are embedded in the CM119A, including dual DAC and earphone driver, ADC, microphone booster, PLL, regulator and USB transceiver modules. It also supports 8 GPIO pins and a buzzer output pin for VoIP applications, and audio adjustments are easily controlled via specific HID-compliant volume control pins. As well, many features are programmable with jumper pins or by external EEPROM. Venders can create custom USB VID/PID/product and manufacturer strings in EEPROM for VoIP software authentications. Creating an Individual phone number for each device is also possible via serial number stored in an external EEPROM.

FEATURES

- Supports USB 2.0 Full Speed operation
- Compliant with USB audio device class specification v1.0
- Supports USB suspend/resume modes and remote wakeup with volume control pins
- Single 12MHz crystal input with on-chip PLL and embedded USB transceiver
- Jumper pin for speaker mode (playback only) or headset mode (playback plus recording)
- For headset mode, USB audio function topology has 2 input terminals, 2 output terminals, 1 mixer unit, 1 selector unit, and 3 feature units
- Jumper pin allows for mixer unit enable/disable when in headset mode

BLOCK DIAGRAM



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1 Description and Overview

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The CM119A is a highly integrated single-chip USB audio controller specifically designed for VoIP (Voice over Internet Protocol) applications. All essential analog modules are embedded in the CM119A, including dual DAC and earphone driver, ADC, microphone booster, PLL, regulator and USB transceiver modules. It also supports 8 GPIO pins and a buzzer output pin for VoIP applications, and audio adjustments are easily controlled via specific HID-compliant volume control pins. As well, many features are programmable with jumper pins or by external EEPROM. Venders can create custom USB VID/PID/product and manufacturer strings in EEPROM for VoIP software authentications. Creating an Individual phone number for each device is also possible via serial number stored in an external EEPROM. Moreover, the CM119A has an I2C interface with MCU for LCM integrated and advanced functions.

Due to the fact that VoIP technology can provide free or low-cost calling worldwide, VoIP applications are becoming increasing popular. To provide a VoIP experience that is equal to using a regular phone, and to eliminate the poor sound quality that results from using PC audio, C-Media has developed the CM119A USB controller. This USB controller enables a regular phone, handset or headset to be used via the USB port of any PC. Furthermore, C-Media works closely with OEMs to quickly bring to market new lines of low-cost, high-quality VoIP products.

2 Features

- Supports USB 2.0 full speed operation
- Compliant with USB audio device class specification v1.0
- Supports USB suspend/resume modes and remote wakeup with volume control pins
- Single 12MHz crystal input with on-chip PLL and embedded USB transceiver
- Jumper pin for speaker mode (playback only) or headset mode (playback plus recording)
- For headset mode, USB audio function topology has 2 input terminals, 2 output terminals, 1 mixer unit, 1 selector unit, and 3 feature units
- Jumper pin allows for mixer unit enable/disable when in headset mode
- For speaker mode, USB audio function topology has 1 input terminal, 1 output terminal, and 1 feature unit
- Supports one control endpoint, one isochroous OUT endpoint, one isochroous IN endpoint, and one interrupt IN endpoint
- Alternate zero bandwidth setting for releasing playback bandwidth on USB Bus when device is inactive
- Volume up, volume down, and playback mute pins support USB HID for host control synchronization
- Record mute pin with LED indicator for record mute status
- External EEPROM interface for vendor's USB VID, PID, product and manufacturer string and serial number
- Supports AES/EBU, IEC60958, S/PDIF consumer formats for stereo PCM data at S/PDIF output
- 8 GPIO pins with read/write via HID interface
- Embedded buzzer function controlled by register
- Supports I2C interface for external MCU integration

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- Jumper pin to set the power mode setting
- Isochronous transfer uses adaptive mode with internal PLL for synchronization
- 48K/44.1KHz sampling rate for both playback and recording
- Soft mute function
- Embedded 16-bit audio DAC with earphone phone amplifier
- Host-side data loss noise-reduction function
- Embedded 16-bit ADC input with microphone boost
- Embedded power-on reset block
- Embedded 5V to 3.3V regulator for single external 5V operation
- Compatible with Win XP/Vista/7/8, Linux and Mac OS X without additional drivers
- 48-pin LQFP package
- Optional hardware SDK tool for third-party software development

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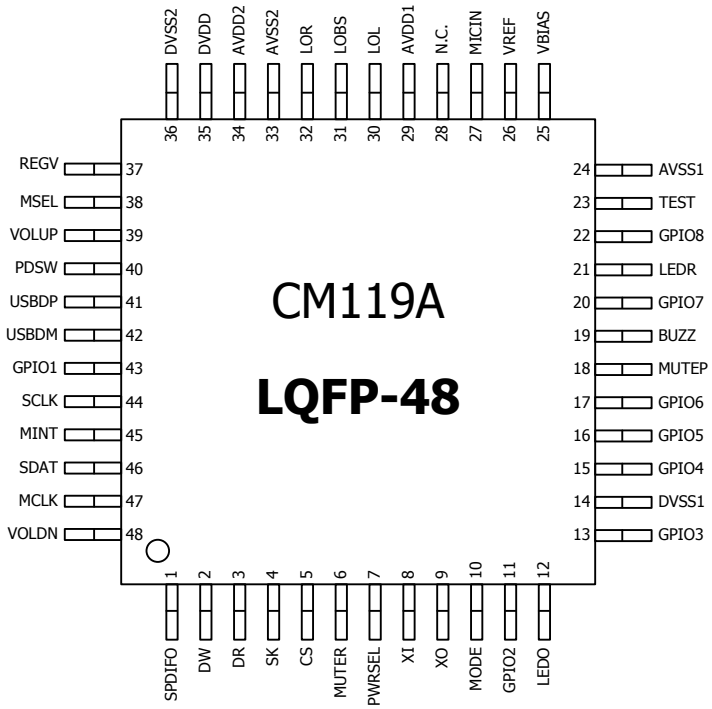
3 Pin Descriptions

3.1 Pin Assignment by Pin Number

Pin #	Signal Name	Pin #	Signal Name	Pin #	Signal Name	Pin #	Signal Name
1	SPDIFO	13	GPIO3	25	VBIAS	37	REGV
2	DW	14	DVSS1	26	VREF	38	MSEL
3	DR	15	GPIO4	27	MICIN	39	VOLUP
4	SK	16	GPIO5	28	N.C.	40	PDSW
5	CS	17	GPIO6	29	AVDD1	41	USBDP
6	MUTER	18	MUTEP	30	LOL	42	USBDM
7	PWRSEL	19	BUZZ	31	LOBS	43	GPIO1
8	XI	20	GPIO7	32	LOR	44	SCLK
9	XO	21	LEDR	33	AVSS2	45	MINT
10	MODE	22	GPIO8	34	AVDD2	46	SDAT
11	GPIO2	23	TEST	35	DVDD	47	MCLK
12	LEDO	24	AVSS1	36	DVSS2	48	VOLDN

3.2 Pin-Out Diagram



Pin Assignments (Top View)

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3.3 Pin Signal Description

Pin #	Symbol	Type	Description
1	SPDIFO	DO, 8mA, SR	SPDIF output
2	DW	DIO, 8mA, PD, 5VT	USB controller data read from EEPROM interface; EEPROM data output
3	DR	DO, 4mA, SR	USB controller data write to EEPROM interface; EEPROM data input
4	SK	DO, 4mA, SR	EEPROM interface clock (100KHz)
5	CS	DO, 4mA, SR	EEPROM interface chip select
6	MUTER	DI, ST, PU	Mute recording (edge trigger with de-bouncing)
7	PWRSEL	DI, ST	H: push up to 3.3V, L: push down to ground Speaker mode – H: 100mA self-powered, L: 500mA Bus-powered Headset mode – H: 100mA Bus-powered, L: 500mA Bus-powered
8	XI	DI	Input pin for 12MHz oscillator
9	XO	DO	Output pin for 12MHz oscillator
10	MODE	DI, ST	H: push up to 3.3V, L: pull down to ground H: speaker mode - playback only L: headset mode - playback & recording
11	GPIO2	DIO, 8mA, PD, 5VT	GPIO pin
12	LEDO	DO, SR, 8mA	LED operation light: output H for power on, toggling for data transmit
13	GPIO3	DIO, 8mA, PD, 5VT	GPIO pin
14	DVSS1	P	Digital grounding
15	GPIO4	DIO, 8mA, PD, 5VT	GPIO pin
16	GPIO5	DIO, 8mA, PD, 5VT	GPIO pin
17	GPIO6	DIO, 8mA, PD, 5VT	GPIO pin
18	MUTEP	DI, ST, PU	Mute playback (edge trigger with de-bouncing)
19	BUZZ	DO, 8mA, SR	Buzzer output pin
20	GPIO7	DIO, 8mA, PD, 5VT	GPIO pin
21	LEDR	DO, SR, 8mA	LED for mute recording indicator, output H when recording is muted
22	GPIO8	DIO, 8mA, PD, 5VT	GPIO pin
23	TEST	DI, ST, PD	Test mode select pin, H: test mode L: normal operation
24	AVSS1	P	Analog ground
25	VBIAS	AO	Microphone bias voltage supply (4.5V)
26	VREF	AO	Connects to external decoupling capacitor for embedded bandgap circuit, 2.25V output
27	MICIN	AI	Microphone input

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Pin #	Symbol	Type	Description
28	N.C.	--	N.C.
29	AVDD1	P	5V analog power for analog circuit
30	LOL	AO	Line out: left channel
31	LOBS	AO	DC 2.25V output for line out bias
32	LOR	AO	Line out right channel
33	AVSS2	P	Analog ground
34	AVDD2	P	5V analog power for analog circuit
35	DVDD	P	5V power supply to internal regulator
36	DVSS2	P	Digital grounding
37	REGV	AO	3.3V reference output for internal 5V Æ 3.3V regulator
38	MSEL	DI, ST	Mixer enable select, worked by MODE pin, H: with mixer/AA-path enabled (with default mute) L: without mixer/AA-path disabled (H: push up to 3.3V, L: push down to ground) USB descriptors will also be changed accordingly
39	VOLUP	DI, ST, PU	Volume up (edge trigger with de-bouncing)
40	PDSW	DO, 4mA , OD	Power down switch control (for PMOS polarity) 0: normal mode, 1: power down mode
41	USBDP	AIO	USB Data D+
42	USBDM	AIO	USB Data D-
43	GPIO1	DIO, 8mA, PD, 5VT	GPIO pin
44	SCLK	DIO, 8mA, PD, 5VT	External MCU serial Bus clock pin
45	MINT	DO, 4mA, SR	External MCU interrupt pin: When register address 4~7 has new data, MINT is set to low; After MCU read MINT is reset to H
46	SDAT	DIO, 8mA, PD, 5VT	External MCU serial bus data pin
47	MCLK	DO, 4mA, SR	External MCU clock pin, clock frequency is programmable Default is 1.5 MHz (options include: 6MHz, 3MHz, 1.5MHz)
48	VOLDN	DI, ST, PU	Volume down (edge trigger with de-bouncing)

Note: DI - Digital Input Pad, DO - Digital Output Pad, DIO - Digital Bi-directional Pad, AI/AO/AIO - Analog Pad, SR Slew Rate Control, ST - Schmitt Trigger, PD/PU - Pull Down or Pull Up, 5VT - 5-volt Tolerant (3.3V Pad), OD - Open Drain

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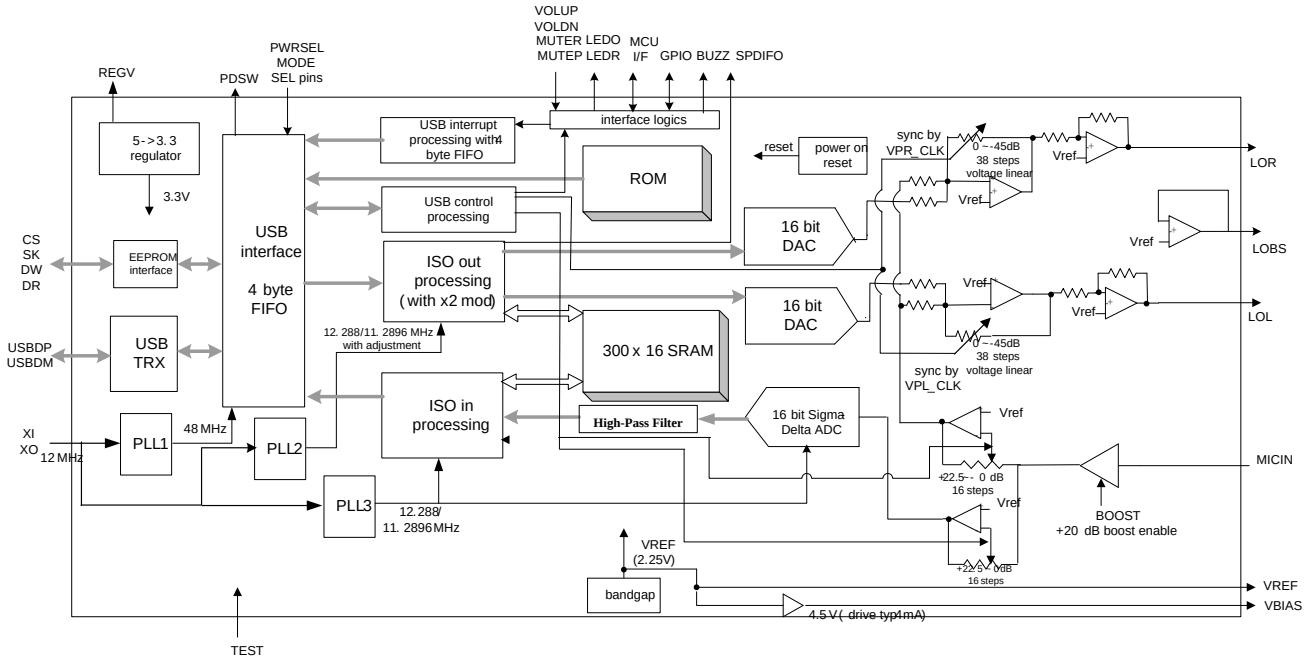
4 MCU Interface

The CM119A has a serial MCU interface that grants access to external MCUs, allowing them to access internal registers. Bi-directional communication between the MCU and host-side software can also occur. This interface offers the flexibility needed for external module control and integration, such as that needed for LCD panels.

5 Block Diagram



CM119A Block Diagram

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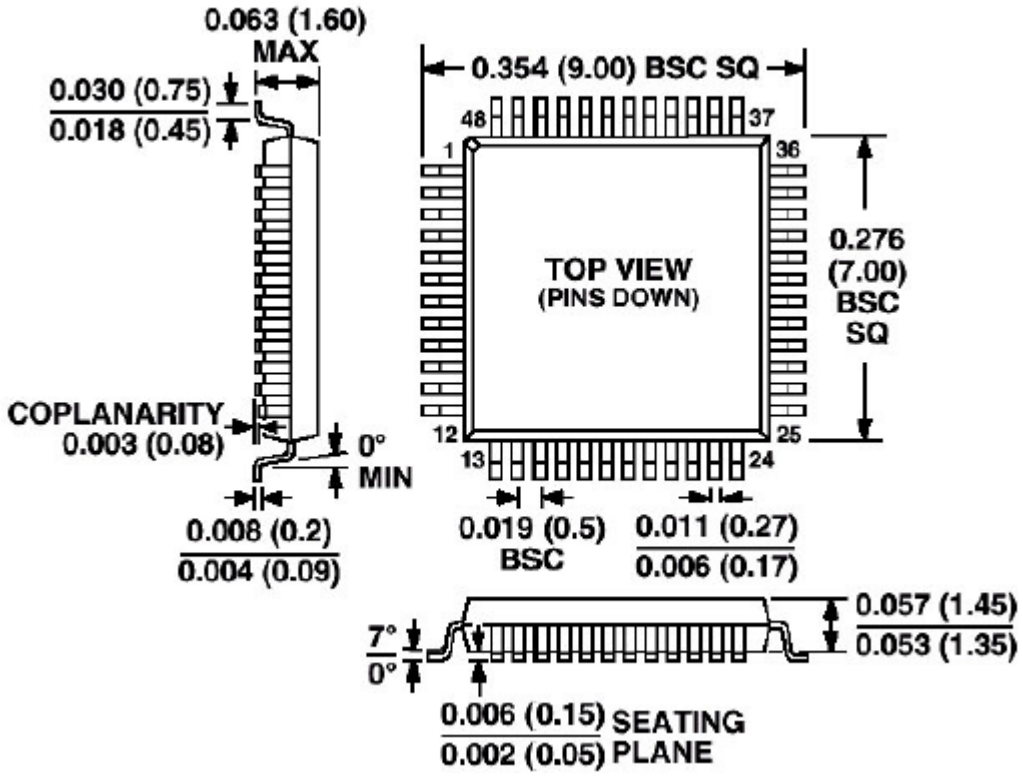
6 Ordering Information

Model Number	Package	Operating Ambient Temperature	Supply Range
CM119A	48-pin LQFP, 7mm × 7mm × 1.4mm (plastic)	0°C to +70°C	DVdd = 5V, AVdd = 5V

Outline Dimensions: Dimensions shown in inches and millimeters

48-Lead Thin Plastic Quad Flatpack (LQFP)



CM119A Ordering Information

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7 Function Description

7.1 USB Interface

The CM119A integrates USB transceiver, PLL and regulator modules, meaning only a few passive components are necessary for USB interface connection. Default USB descriptors are embedded in the CM119A, so no additional design effort is needed for generic USB operation. For custom orders, customers can attach a 93C46 EEPROM to override the embedded VID, PID, product and manufacturer strings, and serial number for each set. The CM119A automatically detects the 93C46, and the overwrite function is performed at start up.

7.1.1 Device Descriptor

Offset	Field	Size	Value (Hex)	Description
0	bLength	1	12	Total: 18 bytes
1	bDescriptorType	1	01	Device descriptor
2	bcdUSB	2	0110	USB 1.1-compliant
4	bDeviceClass	1	00	
5	bDeviceSubClass	1	00	
6	bDeviceProtocol	1	00	
7	bMaxPacketSize0	1	40	Endpoint zero size = 64 bytes
8	idVendor	2	0D8C	Vendor ID
10	idProduct	2	013A	Product ID programmable by MSEL and MODE pin
12	bcdDevice	2	0100	Device compliant with Audio Device class specification version 1.0
14	iManufacturer	1	01	String descriptor index describes manufacturer
15	iProduct	1	02	String descriptor index describes product
16	iSerialNumber	1	03	String descriptor index displays device serial no.
17	bNumConfigurations	1	01	Configuration number = 1

Note: VID, PID, and serial number can be overridden by external EEPROM content

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7.1.2 Configuration Descriptor

Offset	Field	Size	Value (Hex)	Description
0	bLength	1	09	Total: 9 bytes
1	bDescriptorType	1	02	Configuration descriptor
2	wTotalLength	2		Total length of data returned for this configuration, programmable by MSEL and MODE pin
4	bNumInterfaces	1	04 or 03	Number of interfaces supported by this configuration, changed by MODE pin: EP0: control interface EP1: ISO-OUT interface EP2: ISO-IN interface (optional) EP3: INT-IN (HID) interface
5	bConfigurationValue	1	01	
6	iConfiguration	1	00	
7	bmAttributes	1	A0 or E0	Programmable by PWRSEL
8	bMaxPower	2	32 or FA	Maximum power consumption of the USB, programmable by MODE and PWRSEL pins

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7.1.3 Content Format for 93C46

Addr (Dec)	Addr (Hex)	Description	
0	0x00	Magic Word 0x670X where X = bit 4, 3, 2, 1 bit 3, value within address 0x2A,0x2B is valid 1: valid 0: invalid bit 2, manufacture string enable 1: enable(default) 0: disable bit 1, serial number enable control 1: enable 0: disable(default) bit 0, product string enable control 1: enable(default) 0: disable	
1	0x01	VID 2-byte	
2	0x02	PID 2-byte	
3	0x03	Serial number length (low byte)	Serial number first byte (high byte)
4 ~ 9	0x04 ~ 0x09	Serial number: 12 bytes	
10	0x0A	Product string length (low byte)	Product string first byte (high byte)
11 ~ 25	0x0B ~ 0x19	Product string: 30 bytes (default: USB PnP sound device)	
26	0x1A	Manufacturer string length (low byte)	Manufacturer string first byte[t] (high byte)
27 ~ 41	0x1B ~ 0x29	Manufacturer string: 30 bytes (default: C-Media Electronics Inc.)	
42	0x2A	bit 15 ~ 8 DAC initial volume (7-bit) max: 0x02 min: 0x4a bit 7 ~ 0 ADC initial volume (5-bit) max: 0x00 min: 0x78	
43	0x2B	bit 15 ~ bit 9 <reserved> bit 8 Shutdown DAC analog - 1: shutdown, 0: active (default) bit 7 Total power control - 1: enable, 0: disable (default) bit 6 Reserved, should be 0 bit 5 MIC high pass filter - 1: enable (default), 0: disable bit 4 ADC synchronization mode - 1: enable, 0: disable (default) bit 3 MIC BOOST - 1: enable (default), 0: disable bit 2 DAC output terminal property set to SPK or HP 1: Headset, 0: Speaker (default) bit 1 HID - 1: enable (default), 0: disable bit 0 Remote wakeup enable/disable 1: enable, 0: disable (default)	
44 ~ END	0x2C ~ END	<reserved>	

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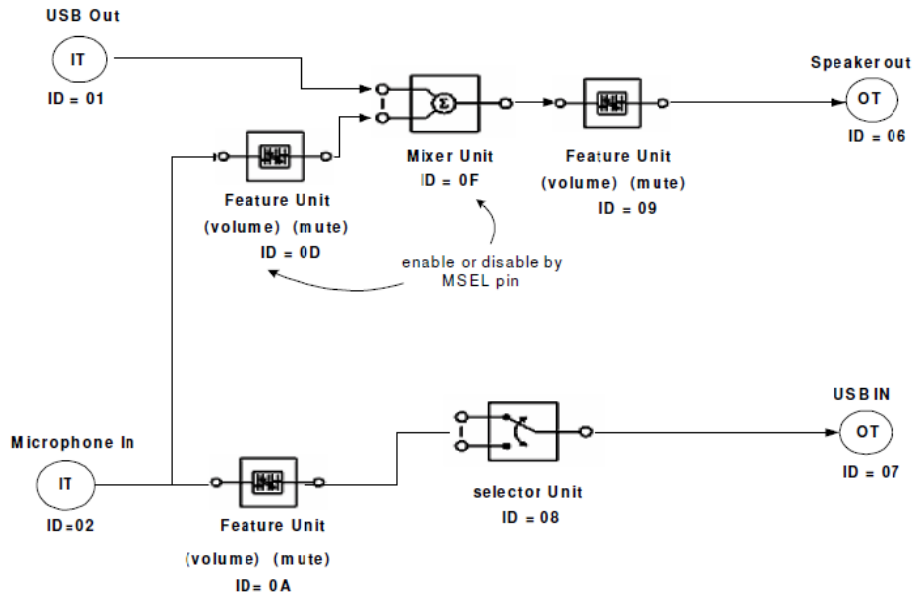
7.1.4 USB Audio Topology Diagram



USB Audio Topology Diagram

7.2 Jumper Pins and Mode Setting

The CM119A can be configured via several jumper pins. These jumper pin settings affect both USB descriptors and USB audio topology. If the MODE pin is pushed up to 3.3V (speaker mode), a playback-only function is activated and no recording function is declared to the host. At this setting, the MSEL pin is ignored and only one input terminal, one output terminal and one feature unit is declared in the USB audio topology.

If the MODE pin is pulled low (headset mode), a full-duplex playback and recording function is reported to the host. The MSEL pin setting activates one mixer unit and one feature unit. The following USB audio topology (7.1.4) is an example of headset mode. The PWRSEL pin affects the power configuration of the CM119A, and together with the MODE pin, there are a total of 4 programmable combinations.

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Combinations		MODE	
		3.3V	GND
PWRSEL	3.3V	Speaker mode: Playback only (100mA self-powered)	Headset mode: Playback and recording (100mA Bus-powered)
	GND	Speaker mode: Playback only (500mA Bus-powered)	Headset mode: Playback and recording (500mA Bus-powered)

7.3 Description of HID Feature

The CM119A's HID feature allows users to set volume up, volume down, playback mute and recording mute button pins, and reports the changes to the host to synchronize host side settings. In addition, all CM119A internal registers can be accessed via HID function call.

USB protocols can configure devices at startup or when they are plugged in at run time. These devices are categorized into various device classes. Each device class defines the common behavior and protocols for devices that serve similar functions. The HID (Human Interface Device) class is one of the device classes.

The HID class consists primarily of devices that are used to control the operation of computer systems. Typical examples of HID class devices include:

- Keyboards and pointing devices: mice, trackballs and joysticks
- Front-panel controls: knobs, switches, buttons and sliders
- Controls that might be found on VCR remote controls, games or simulation devices: data gloves, throttles, and steering wheels
- Devices that may not require human interaction but provide data in a similar format to HID class devices: bar-code readers, thermometers or voltmeters

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7.3.1 HID Descriptors

HID Interface Descriptors

Offset	Field	Size	Value (Hex)	Description
0	bLength	1	09	Size of this descriptor: 9 bytes
1	bDescriptorType	1	04	Interface descriptor type
2	bInterfaceNumber	1	03	Interface number: 3
3	bAlternateSetting	1	00	Alternate: 0
4	bNumEndpoints	1	01	Number of endpoints used by this interface: 1
5	bInterfaceClass	1	03	Interface class: HID
6	bInterfaceSubClass	1	00	Subclass: no
7	bInterfaceProtocol	1	00	Must be set to 0
8	iInterface	1	00	String descriptor index that describes this interface

HID Descriptors

Offset	Field	Size	Value (Hex)	Description
0	bLength	1	09	Total: 9 bytes
1	bDescriptorType	1	21	HID descriptor type
2	bcdHID	2	0100	HID class version 1.0
4	bCountryCode	1	00	
5	bNumDescriptors	1	01	
6	bDescriptorType	1	22	Report descriptor
7	wDescriptorLength	2	0030	Total size of the optional descriptor: 48 bytes

Interrupt IN Endpoint Descriptors

Offset	Field	Size	Value (Hex)	Description
0	bLength	1	07	Total: 7 bytes
1	bDescriptorType	1	05	Endpoint descriptor type
2	bEndpointAddress	1	83	In Endpoint Number = 3
3	bmAttributes	1	03	Interrupt endpoint type
4	wMaxPacketSize	2	0004	Maximum packet size: 4 bytes
6	bInterval	1	2	2ms

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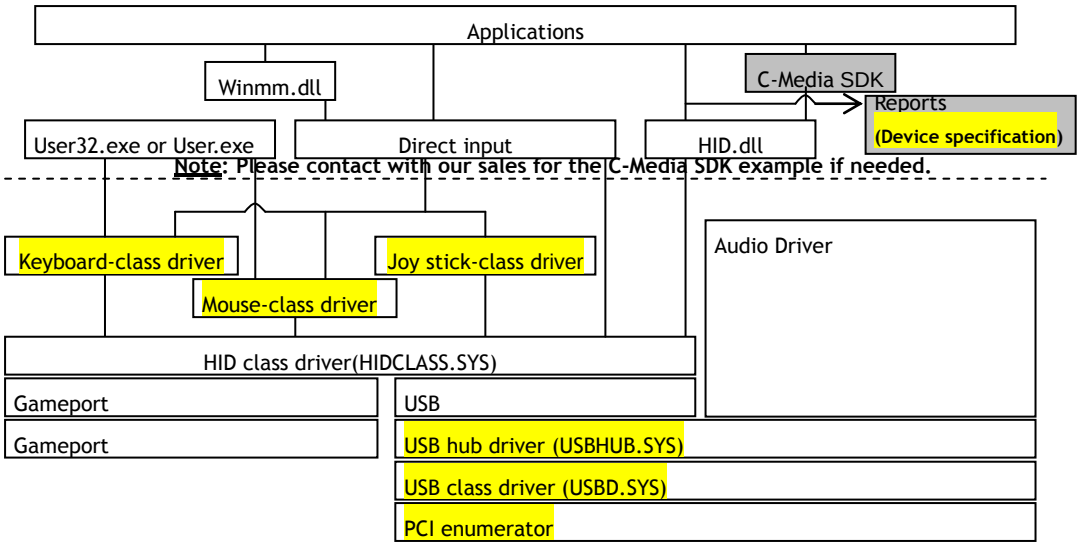
7.3.1 Windows Software Architecture for HID



7.4 Internal Registers

All of CM119A's internal registers can be accessed via generic HID functional calls without the need to develop a kernel mode driver. In total, 4 bytes of data can be read or written from the HID. The input report is for read and the output report is for write. These internal registers of are used to control GPIO pin, S/PDIF output, EEPROM and MCU data access. The host-side HID or external MCU also have access to CM119A's internal registers, allowing for two-way communication to be achieved.

7.4.1 Access via HID Class Command

HID_IR0 to HID_IR3 are the HID input reports used by the host side to receive data from the CM119A. HID_OR0 to HID_OR3 are the HID output reports used by the host side to send data to the CM119A. HID interrupt will occur when HID_IR0-3 is updated by the MCU (and GPI in case of HID_IR0[7:6] == 2'b00).

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HID_IR0 (HID input report byte 0)

Offset: 0x00

Bits	Read/Write	Description	Default
7-6	R	When HID_OR0[7] == 1'b0: HID_IR0-3 are programmed by MCU (and GPI) 0: HID_IR1 is used as GPI 1: HID_IR0-3 are used as generic HID registers 2: values written to HID_IR0-3 are also mapped to MCU_CTRL, EEPROM_DATA0-1 and EEPROM_CTRL 3: reserved	0x0
5-4	R	When HID_OR0[7] == 1'b0: generic registers programmed by MCU When HID_OR0[7] == 1'b1: mapped from MCU_CTRL[5:4]	0x0
3	R	0: no activity on record-mute button 1: record-mute button pressed then released	0x0
2	R	0: no activity on playback-mute button 1: playback-mute button pressed then released	0x0
1	R	0: volume-down button released 1: volume-down button pressed	0x0
0	R	0: volume-up button released 1: volume-up button pressed	0x0

HID_IR1 (HID input report byte 1)

Offset: 0x01

Bits	Read/Write	Description	Default
7-0	R	When HID_OR0[7] == 1'b0: GPI (when HID_IR0[7:6] == 2'b00); or generic registers programmed by MCU (otherwise) When HID_OR0[7] == 1'b1: Mapped from EEPROM_DATA0	0x00

HID_IR2 (HID input report byte 2)

Offset: 0x02

Bits	Read/Write	Description	Default
7-0	R	When HID_OR0[7] == 1'b0: generic registers programmed by MCU When HID_OR0[7] == 1'b1: mapped from EEPROM_DATA1	0x00

HID_IR3 (HID input report byte 3)

Offset: 0x03

Bits	Read/Write	Description	Default
7-0	R	When HID_OR0[7] == 1'b0: generic registers programmed by MCU When HID_OR0[7] == 1'b1: mapped from EEPROM_CTRL	0x00

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HID_OR0 (HID output report byte 0)

Offset: 0x04

Bits	Read/Write	Description	Default
7-6	R/W	0: HID_OR1-2 are used for GPO; HID_OR0-3 are used for buzzer and SPDIF 1: HID_OR0-3 are used as generic HID registers 2: values written to HID_OR0-3 are also mapped to MCU_CTRL, EEPROM_DATA0-1 and EEPROM_CTRL (see note below) 3: reserved	0x0
5	R/W	When HID_OR0[7] == 1'b0, 0: buzzer off, 1: buzzer on When HID_OR0[7] == 1'b1: mapped to MCU_CTRL[5]	0x0
4	R/W	When HID_OR0[7] == 1'b0: valid bit in SPDIF frame When HID_OR0[7] == 1'b1: mapped to MCU_CTRL[4]	0x0
3-0	R/W	When HID_OR0[7] == 1'b0: first nibble of SPDIF status channel When HID_OR0[7] == 1'b1: reserved	0x0

Note : When EEPROM access is done, HID interrupt will occur. USB host can get the result from interrupt endpoint 3.

HID_OR1 (HID output report byte 1)

Offset: 0x05

Bits	Read/Write	Description	Default
7-0	R/W	When HID_OR0[7:6] == 2'b00, 0: GPO drives L, 1: GPO drives H When HID_OR0[7:6] == 2'b01: generic HID registers When HID_OR0[7:6] == 2'b1x: mapped to EEPROM___DATA0	0x00

HID_OR2 (HID output report byte 2)

Offset: 0x06

Bits	Read/Write	Description	Default
7-0	R/W	When HID_OR0[7:6] == 2'b00: 0: set GPIO to input mode 1: set GPIO to output mode When HID_OR0[7:6] == 2'b01: generic HID registers When HID_OR0[7:6] == 2'b1x: mapped to EEPROM_DATA1	0x00

HID_OR3 (HID output report byte 3)

Offset: 0x07

Bits	Read/Write	Description	Default
7-0	R/W	When HID_OR0[7] == 1'b0: category byte of SPDIF status channel When HID_OR0[7] == 1'b1: mapped to EEPROM_CTRL	0x00

Note: HID_OR3 is used for SPDIF when SPDIF_CONFIG[5] == 1'b0

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7.4.2 Access via External Serial Interface by MCU

The external MCU can write data to HID_IR0 to HID_IR3 and read data from HID_OR0 to HID_OR3. MINT is active when HID_OR0-3 is updated by the Set_Output_Report HID class command, and will be cleared after HID_OR0-3 is read by MCU.

HID_IR0 (HID input report byte 0)

Offset: 0x00

Bits	Read/Write	Description	Default
7-6	R/W	0: HID_IR0-3 is not used by MCU 1: HID_IR0-3 is used as generic HID register 2: values written to HID_IR0-3 are also mapped to MCU_CTRL, EEPROM_DATA0-1 and EEPROM_CTRL (see Note) 3: reserved	0x0
5	R/W	When HID_IR0[7] == 1'b0, 0: buzzer off, 1: buzzer on When HID_IR0[7] == 1'b1: mapped to MCU_CTRL[5]	0x0
4	R/W	When HID_IR0[7] == 1'b0: generic HID register When HID_IR0[7] == 1'b1: mapped to MCU_CTRL[4]	0x0
3	R	0: no activity on record-mute button 1: record-mute button pressed then released	0x0
2	R	0: no activity on playback-mute button 1: playback-mute button pressed then released	0x0
1	R	0: volume-down button released 1: volume-down button pressed	0x0
0	R	0: volume-up button released 1: volume-up button pressed	0x0

Note: When EEPROM access is done, MINT will be active. Once MCU reads HID_OR0-3, MINT will be cleared

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HID_IR1 (HID input report byte 1)

Offset: 0x01

Bits	Read/Write	Description	Default
7-0	R/W	When HID_IR0[7] == 1'b0: generic HID registers When HID_IR0[7] == 1'b1: mapped to EEPROM_DATA0	0x00

HID_IR2 (HID input report byte 2)

Offset: 0x02

Bits	Read/Write	Description	Default
7-0	R/W	When HID_IR0[7] == 1'b0: generic HID registers When HID_IR0[7] == 1'b1: mapped to EEPROM_DATA1	0x00

HID_IR3 (HID input report byte 3)

Offset: 0x03

Bits	Read/Write	Description	Default
7-0	R/W	When HID_IR0[7] == 1'b0: generic HID registers When HID_IR0[7] == 1'b1: mapped to EEPROM_CTRL	0x00

HID_OR0 (HID output report byte 0)

Offset: 0x04

Bits	Read/Write	Description	Default
7-6	R	When HID_IR0[7] == 1'b0: HID_OR0-3 are programmed by USB host 0: HID_OR1-2 are used for GPO 1: HID_OR0-3 are used as generic HID registers 2: values written to HID_OR0-3 are also mapped to MCU_CTRL, EEPROM_DATA0-1 and EEPROM_CTRL 3: reserved When HID_IR0[7] == 1'b1: Always 2'b11	0x0
5-4	R	When HID_IR0[7] == 1'b0: generic registers programmed by USB host When HID_IR0[7] == 1'b1: mapped from MCU_CTRL[5:4]	0x0
3-0	R	When HID_IR0[7] == 1'b0: generic registers programmed by USB host When HID_IR0[7] == 1'b1: always 4'h0	0x0

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HID_OR1 (HID output report byte 1)

Offset: 0x05

Bits	Read/Write	Description	Default
7-0	R	When HID_IR0[7] == 1'b0: generic registers programmed by USB host When HID_IR0[7] == 1'b1: mapped from EEPROM_DATA0	0x00

HID_OR2 (HID output report byte 2)

Offset: 0x06

Bits	Read/Write	Description	Default
7-0	R	When HID_IR0[7] == 1'b0: generic registers programmed by USB host When HID_IR0[7] == 1'b1: mapped from EEPROM_DATA1	

HID_OR3 (HID output report byte 3)

Offset: 0x07

Bits	Read/Write	Description	Default
7-0	R	When HID_IR0[7] == 1'b0: generic registers programmed by USB host When HID_IR0[7] == 1'b1: mapped from EEPROM_CTRL	0x00

7.4.3 Indirect Accessed Registers

MCU_CTRL (MCU control)

Offset: 0x08

Bits	Read/Write	Description	Default
7-6	--	Reserved	0x0
5-4	R/W	0: MCLK operating at 1.5MHz 1: MCLK operating at 3MHz 2: MCLK operating at 6MHz 3: reserved	0x0
3-0	--	Reserved	0x0

EEPROM_DATA0 (Low byte of EEPROM data)

Offset: 0x09

Bits	Read/Write	Description	Default
7-0	R/W	Low byte of EEPROM data to be accessed	0x00

EEPROM_DATA1 (High byte of EEPROM data)

Offset: 0x0a

Bits	Read/Write	Description	Default
7-0	R/W	High byte of EEPROM data to be accessed	0x00

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EEPROM_CTRL (Serial EEPROM access control)

Offset: 0x0b

Bits	Read/Write	Description	Default
7	R/W	When register reads, 0: no EEPROM access pending, 1: last EEPROM access pending When register writes, 0: no action, 1: start EEPROM access (will clear to 0 automatically)	0x0
6	R/W	0: read EEPROM 1: write EEPROM	0x0
5-0	R/W	Address of serial EEPROM	0x00

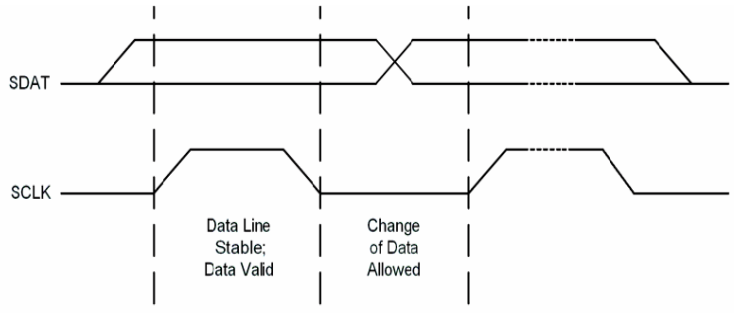
7.5 MCU Interface

On the MCU serial interface, the CM119A serves as a slave device with bit rate up to 400Kbps (fast mode). The MCU can read/write 3 bytes to the CM119A device using a 2-bit register address. Since the host side and MCU both have access to all the internal registers, access contention when both host and MCU try to access the same register should be avoided upon application. The CM119A's 7-bit slave address is assigned as 7'b0111000.

When one byte of data is written by the MCU, the CM119A will transfer a total of 4 bytes to the USB host via an additional interrupt pipe. The sequence of the upward HID report is button status first (address 00), then register with address 01, then register with address 02, then register with address 03. The USB host will keep polling the upward HID report every 2mS. When any button is pressed or released, or there is incoming MCU data, the CM119A will transfer the 4 bytes of HID report to the USB host.

The CM119A can also transfer one byte of MCU data from the USB host to its register.This is accomplished by a 'Set Output Report' HID class request via the default control pipe. The MCU can get this downward byte by interrupt or polling.

The CM119A has one input pin (SCLK) that receives serial clock data from the MCU, and one open-drain output pin (SDAT) that sends or receives serial signals to/from MCU. As shown below, SDAT should be stable when SCLK is high, and can have transition only when 'SCLK' is low.



Bit Transfer on the MCU Interface

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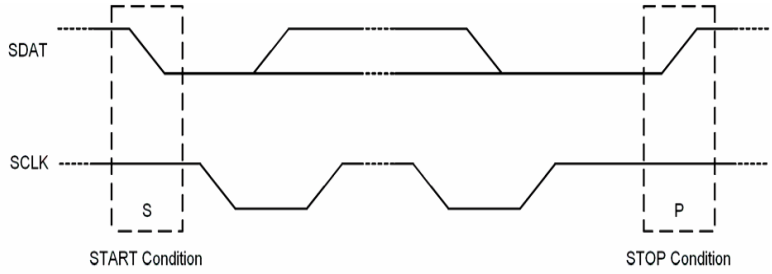
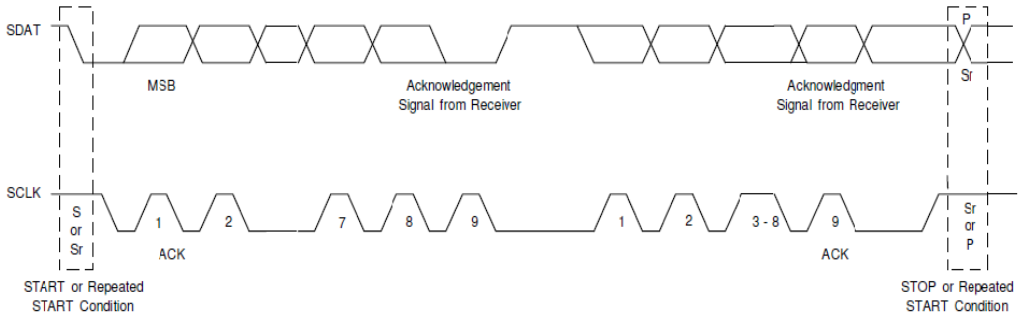
START and STOP conditions shown below are the exception. Every transaction begins from a START, and ends with a STOP, or another START (repeated START).

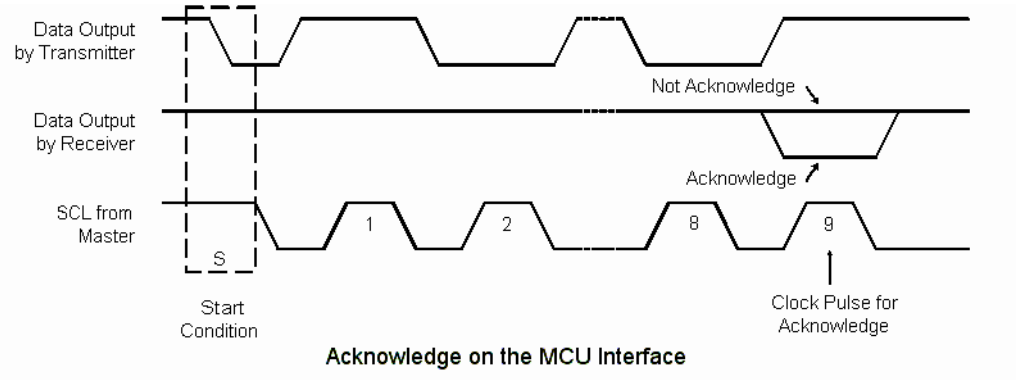


START and STOP Conditions

The figure below demonstrates a typical transaction. After every 8 bits sent by the transmitter, the receiver should send one bit low for positive acknowledgement or one bit high for negative acknowledgement. After the negative acknowledgement, a STOP or repeated START should follow. The next figure shows more details regarding the acknowledgement bit. Note, that SCLK is always driven by the master.



Data Transfer on the MCU Interface



Acknowledge on the MCU Interface

The figure below shows a complete data transfer. After a START, the MCU should send a 7-bit slave address (7'b0111000) first, with the 8th bit denoting a read transfer when it's high, or a write transfer when it's low. The first acknowledgement always comes from the CM119A.

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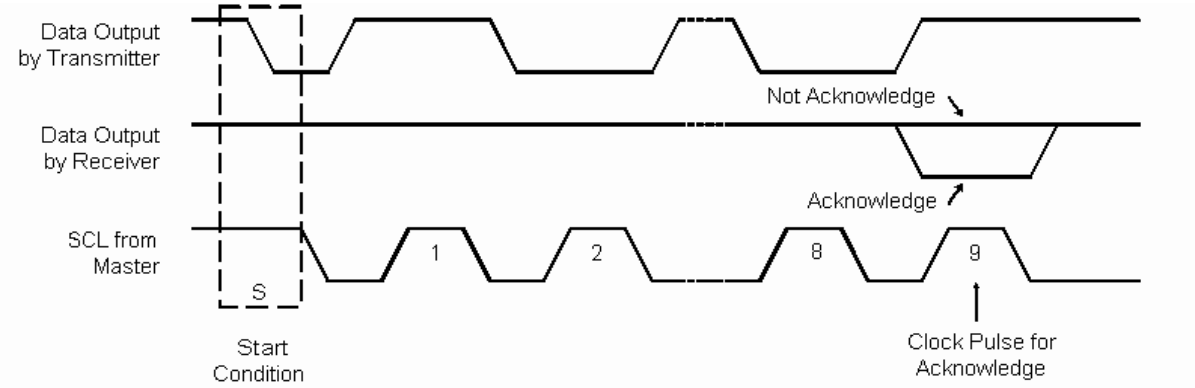
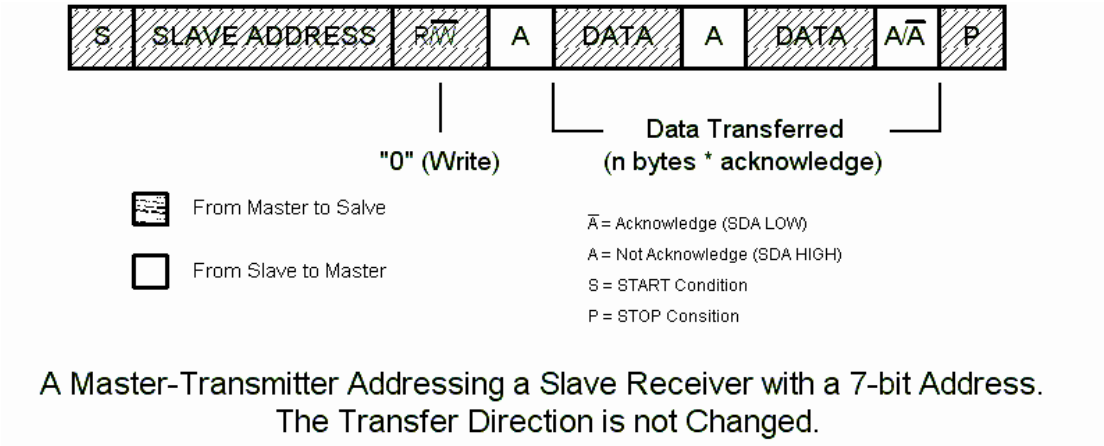


Acknowledge on the MCU Interface

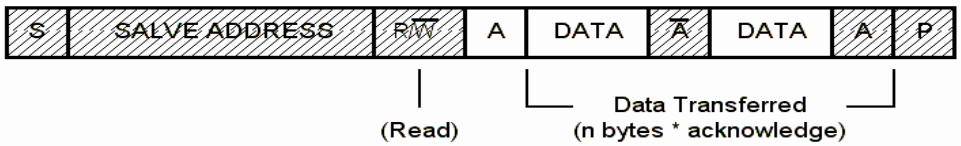
During the write transfer, the MCU continues acting as the master, and the transfer direction is not changed. The following figure gives an example of one byte write transfer.



A Master-Transmitter Addressing a Slave Receiver with a 7-bit Address.
The Transfer Direction is not Changed.

The CM119A regards the first data byte as the register address. The second data byte is the content that MCU writes at the register address. If there is the third data byte, CM119A will auto-increment this byte to the next register address.

The figure below shows an example of a two-byte read transfer. Because the CM119A has an auto-increment function, the second byte of data will be the register data on the next address.



A Master reads a Salve immediately after the first Byte

Please note the USB host tries to get new HID data every 2mS. If the continuous write transfers are too close

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together in time, the preceding transfer may have no effect.

The figure below shows typical transactions between the MCU and the CM119A. After a START, the MCU should first send a 7-bit slave address (0111000), and then an 8th bit that denotes a read transfer when it's high, or a write transfer when it's low.

MCU write:

S	0x70	0	0x00	0	Byte 0	0	Byte 1	0	Byte 2	0	Byte 3	0	P

MCU read:

S	0x70	0	0x04	0									
S	0x71	0	Byte 0	0	Byte 1	0	Byte 2	0	Byte 3	1	P		

	From CM119A to MCU		From MCU to CM119A
S	START condition	P	STOP condition
0	Positive acknowledge	1	Negative acknowledge
Byte n	One byte data (address n)		

During a write transfer, the MCU acts as the transmitter. The CM119A will regard the first byte of data received as the start register address. The following four bytes are the content to be written to the register addresses. In a read transfer, two transactions are necessary. The first transaction from the MCU will reset the start register address. Then, the MCU will receive four bytes of data during the second transaction.

Note 1: Bits 0~3 of the first HID byte always reflect button activity, so they can not be written by the MCU

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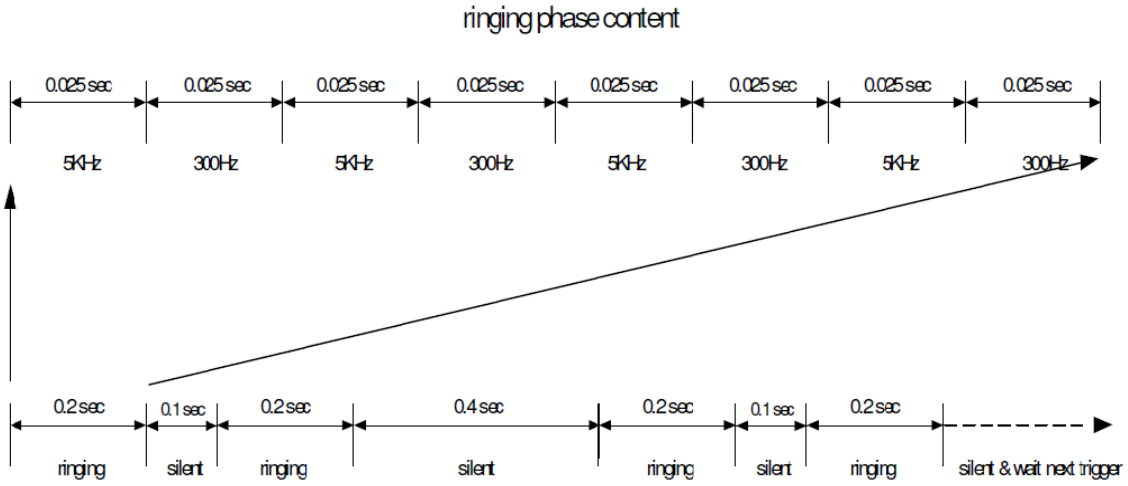
7.6 Buzzer Output

Each time the software sets the register HID-OR0 bit 5 to “1”, an embedded ringing sequence is played once. Since the delay between one sequence and next sequence is quite long (approx. 1 ~ 2 seconds), the H/W will play only one sequence and then stop to write to the register.



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8 Electrical Characteristics

8.1 Absolute Maximum Rating

Symbol	Parameter	Value	Unit
Dvmin	Min. digital supply voltage	- 0.3	V
Dvmax	Max digital supply voltage	+ 6	V
Avmin	Min analog supply voltage	- 0.3	V
Avmax	Max analog supply voltage	+ 6	V
Dvinout	Voltage on any digital input or Output pin	-0.3 to +5.5	V
Avinout	Voltage on any analog input or Output pin	-0.3 to +5.5	V
T_{stg}	Storage temperature range	-40 to +125	^0C
ESD (HBM)	ESD human body mode	4000	V
ESD (MM)	ESD machine mode	200	V

8.2 Operation Conditions

Operation Conditions				
	Min.	**Typ**	**Max.**	**Unit**
Analog Supply Voltage	4.5	5.0	5.5	V
Digital Supply Voltage	4.5	5.0	5.5	V
Total Power Consumption	-	35	-	mA
Suspend Mode Power Consumption	-	320	-	uA
Operating ambient temperature	0	-	70	^0C

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8.3 Electrical Parameters

	Min.	Typ	Max.	Unit
DAC (10K Ohm Loading)				
Resolution	-	16	-	Bits
THD + N (-3dBr)	-	-74.29	-	dB
SNR	-	93.6	-	dB
Silent SNR	-	98.2	-	dB
Dynamic range	-	93.8	-	dB
Frequency response 48KHz	20	-	20K	Hz
Frequency response 44.1KHz	20	-	20K	Hz
Output voltage (rms)	-	1.25	-	Vrms
Output voltage swing	0.5	-	4.0	V
ADC				
Resolution	-	16	-	bit
THD + N (-3dBr)	-	-76.1	-	dB
SNR	-	83.1	-	dB
Dynamic range	-	81.6	-	dB
Frequency response 48KHz	20	-	19.2K	Hz
Frequency response 44.1KHz	20	-	17.6K	Hz
Input range	0	-	2.88	Vpp
Amplification				
Volume control level	-45	-	0	dB
Volume control step	-	38	-	Steps
Microphone Input				
Boost gain	-	+22.5	-	dB
Gain adjustment range	0	-	22.5	dB
Gain adjustment steps	-	16	-	Steps
Mixer gain adjustment	-33.0	-	12.0	dB
Mixer gain adjustment steps	-	32	-	Steps

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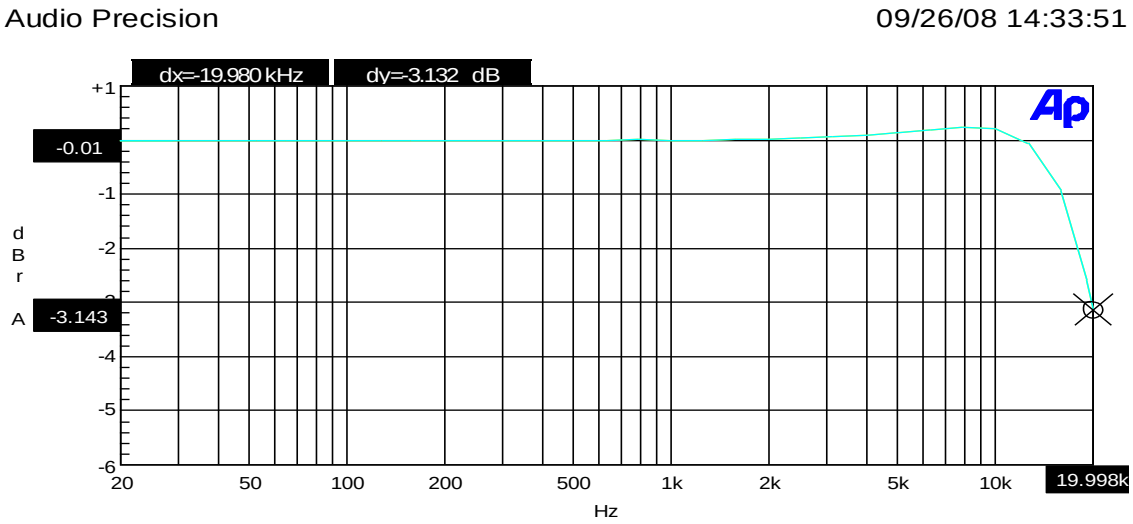
9 Frequency Response Graphs

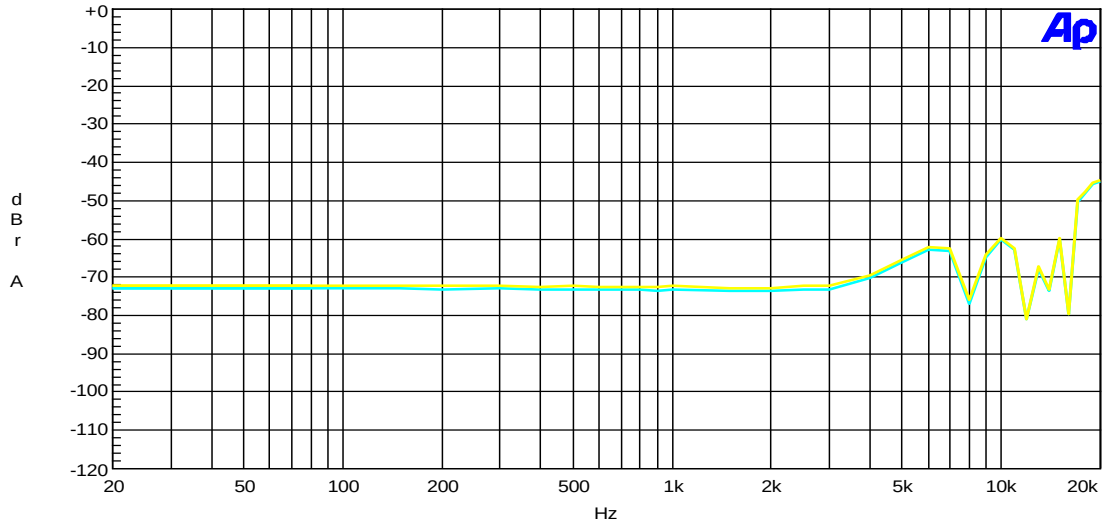
9.1 Line Out Frequency Response @ 48KHz Sample Rate (10K Ohm Loading)



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Cyan	Solid	1	Fasttest.Ch.1 Ampl!Normalize	Left	
1	2	Yellow	Solid	1	Fasttest.Ch.2 Ampl!Normalize	Left	

Vista-Frequency Response-M48k.at27

9.2 Line Out THD+N @ 48KHz sample rate (10K Ohm Loading)



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Cyan	Solid	2	Anlr.THD+N Ampl	Left	
1	2	Yellow	Solid	2	Anlr.THD+N Ampl	Left	

Vista-D-A THD+N.at27

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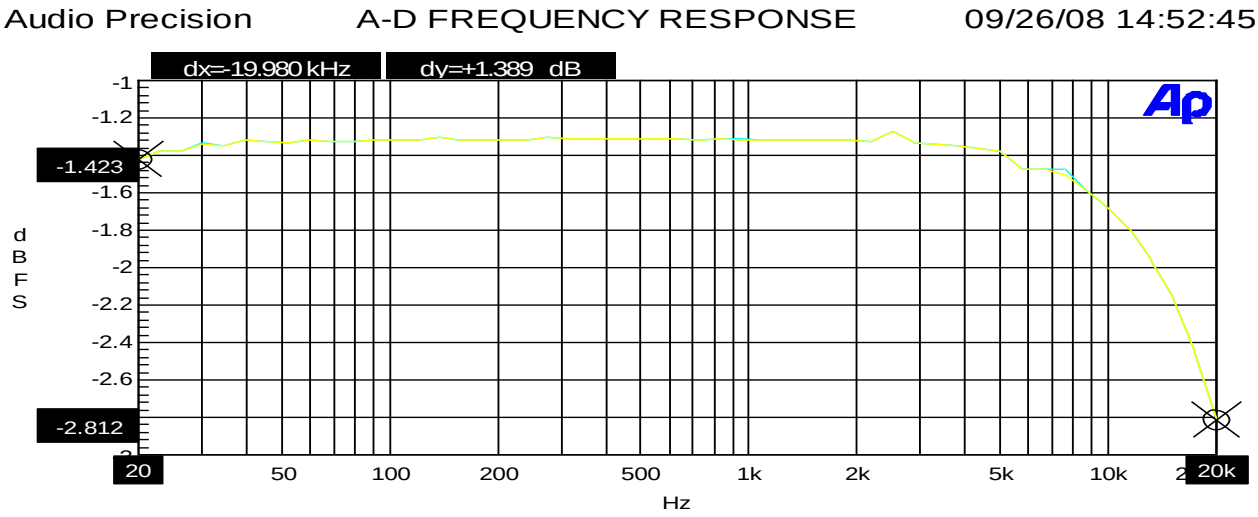
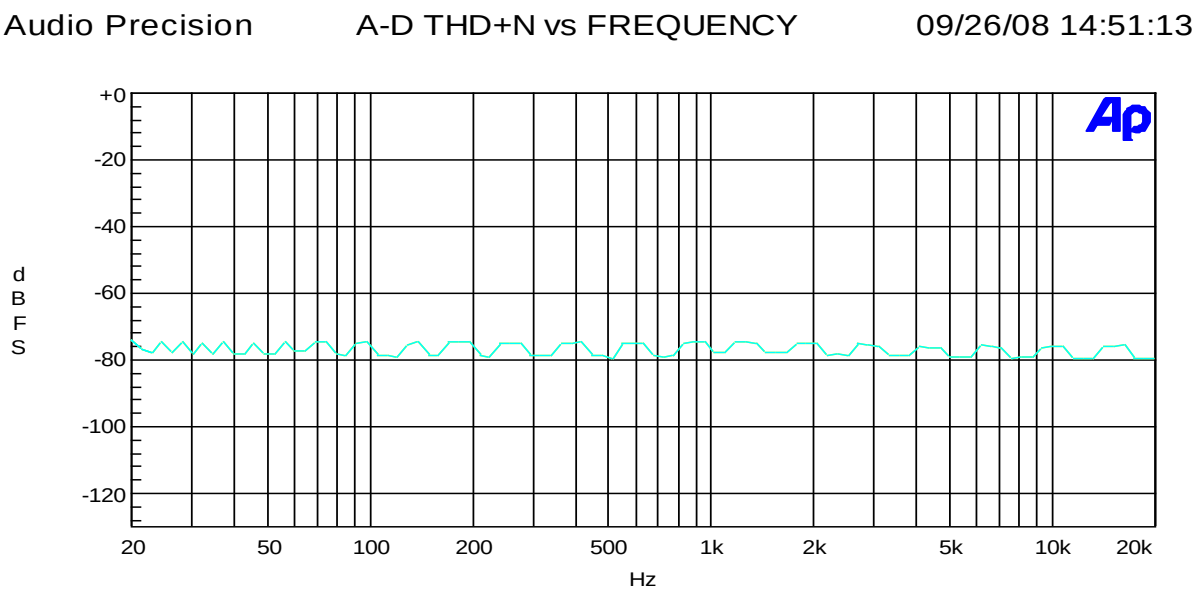
9.3 Microphone Input Frequency Response @ 48KHz Sample Rate



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment	Cursor1
1	1	Yellow	Solid	1	DSP Anlr.Level A	Left		*-2.812 dBFS
1	2	Cyan	Solid	1	DSP Anlr.Level B	Left		-2.812 dBFS

Vista-A-D Frequency Response.at2c

9.4 Microphone InP put THD+N @ 48KHz Sample Rate



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Yellow	Solid	1	DSP Anlr.THD+N Ampl A	Left	
1	2	Cyan	Solid	1	DSP Anlr.THD+N Ampl B	Left	

Vista-A-D THD+N.at2c

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Reference

- USB-IF & USB specification 1.1 and 2.0-compliant
- USB audio device class specification 1.0-compliant
- USB human interface device class specification 1.11-compliant

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—End of Datasheet—

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